REMARKS

In the December 10, 1999 Office Action, the Examiner rejected claims 16-27 pending in the application. After entry of the foregoing amendments, claims 16-33 are pending in the application. Reconsideration of the previously pending claims 16-27 and allowance of all claims 16-33 is earnestly requested.

Claims 16-21 and 23-27 stand rejected under 35 U.S.C. § 103 as being unpatentable over purportedly admitted prior art in view of United States Patent Number 5,886,410, issued to Chiang *et. al.* on March 23, 1999 (hereinafter "Chiang *et al.*"). More particularly, the Examiner states that the purportedly admitted prior art does not teach a protective layer disposed on top of the low-k material, wherein said the protective layer has openings for allowing the metal in the vias to contact the first metal lines, but that Chiang *et al.* teaches an interconnect structure having a protection layer disposed on top of the low-k material layer, wherein the protection layer has openings for allowing metal in the vias to contact the metal lines. Applicants respectfully traverse this rejection. In particular, Applicants submit that even if the cited references teach or suggest the elements recited by the Examiner, such references do not teach each and every element of Applicants' claimed invention. Furthermore, as discussed in greater detail below, nothing in either reference suggests combining the purportedly admitted prior art, which discloses a low-k material formed between metal line and a silicon oxide film formed over the low-k film with Chiang *et al.*, which discloses a low-k material covered by a hard mask dielectric material.

Chiang *et. al.* generally discloses an interconnect structure including a low-k dielectric feature formed between metal lines and a hard mark deposited onto the low-k material. Chiang *et al.* further discloses depositing metal over the hard mask material to form additional metal lines.

Applicants' claimed invention, as set forth in claim 16 and claims 17-27 that depend therefrom, includes at least three distinct layers: a "low-k material filling the gaps between the metal lines", a "protective layer", and a "dielectric layer formed over the protective layer." In

contrast, the purportedly admitted prior art does not include a "protective layer" and Chiang *et al.* does not disclose "a dielectric layer formed over the protective layer." Thus, each reference does not include at least one element—*e.g.*, layer—found in Applicants' claimed invention. Indeed, when an interconnect structure in accordance with Chiang *et al.* includes hard mask material consisting of silicon dioxide (disclosed at column 4, line 6) and the distance between a top of a metal line and the bottom of the hard mask material is zero (disclosed at column 4, line 26) the interconnect structures disclosed in the admitted prior art and Chiang *et al.* are essentially the same. That is, both references teach a structure having a low-k material topped with another dielectric material. Thus, no combination of these references teach or suggest the an interconnect structure having a "low-k material filling the gaps between the metal lines", a "protective layer", and a "dielectric layer formed over the protective layer" as set forth in Applicants' claim 16 and claims 17-27 that depend therefrom.

In addition to the arguments set forth above, Applicants submit that nothing in either the allegedly admitted prior art, Chiang *et al.*, or a combination of these references teaches or suggests "a protective layer formed over the metal lines and the low-k material, wherein the protective layer covers at least one *vertical portion* of the low-k material" (emphasis added) as set forth in claim 16, from which claims 17-27 depend." Rather, Chiang *et al.* discloses forming an interconnect structure by depositing low-k material over metal lines, depositing the hard mark material over the low-k material, etching through the hard mask material, and then using the etched hard mask material as a template to etch the low-k material. Forming a device using this method would not produce "a protective layer formed over the metal lines and the low-k material, wherein the protective layer covers at least one *vertical portion* of the low-k material" (emphasis added) as set forth in claim 16. Accordingly, Applicants submit that claims 16-27 are patentable over the allegedly admitted prior art, Chiang *et al.*, or a combination of these references, and Applicants therefore earnestly solicit allowance of claims 16-27.

Claim 22 stands rejected under 35 U.S.C. §103 as being unpatentable over Chiang *et al.* as applied to claims 16-21, in further view of United States Patent No. 5,317,192, issued to Chen *et al.* on May 31, 1994 (hereinafter "Chen *et al.*"). Applicants respectfully traverse this rejection

because nothing in either reference suggests combing the references, and moreover, a combination of these references does not teach or suggest Applicants' claimed invention.

Chen *et al.* discloses an integrated circuit contact structure including a conductive region, a conformal insulating layer, a planarizing insulating layer, thin barrier sidewalls, and a conductive metal layer. Chen *et al.* does not disclose use of "low-k material" or "a dielectric layer formed over the protective layer."

Neither Chiang *et al.* nor a combination of Chiang *et al.* with purportedly admitted prior art teaches or suggests "a protective layer formed over the metal lines and the low-k material, wherein the protective layer covers at least one vertical portion of the low-k material" as set forth in claim 16, from which claim 22 depends. Further, no combination of any of the references: purportedly admitted prior art, Chiang *et al.*, and Chen *et al.* teaches or suggests "[t]he interconnect of claim 16, further comprising a spacer disposed on the *vertical portion of the low-k material* in the vias" (emphasis added) as set forth in claim 22.

In addition, as noted above, nothing in either Chiang *et al.* or Chen *et al.* suggests combing the references. Specifically, Chen *et al.* discloses forming barrier sidewalls to protect metal layer 30 from impurities contained within planarizing insulating layer 16 (column 3, line 2). The interconnect structures disclosed in Chiang *et al.* do not include a planarizing insulating layer. Thus, it would not be obvious to combine the sidewall of Chen *et al.* with the interconnect structure disclosed in Chiang *et al.*, because problems resolved with the spacer of Chen *et al.* may not be present in the interconnect structures of Chiang *et al.* Accordingly, Applicants submit that claim 22 is independently allowable over the cited references.

Similarly, new claims 28-33 are allowable over the cited references because none of the cited references, alone or in any combination, teach or disclose "a protective layer interposed between said low-k dielectric structures and said second dielectric material" as set forth in claim 28, from which claims 29-33 depend. In particular, none of the references suggest placing a protective layer *between* a low-k dielectric structure and a second dielectric material. Accordingly, Applicants submit that claims 28-33 are allowable over the cited references and earnestly request allowance of claims 28-33.

Should the Examiner have any questions regarding this Response and Amendment or feel that a telephone call to the undersigned would be helpful, the Examiner is invited to call the undersigned at the number listed below.

Respectfully submitted,

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